What is claimed is:

1. A pulse generator having a comparator whose output is generated in response to a difference between a potential level of a ramp signal from a ramp signal generator and a potential level of a threshold signal from a threshold signal generator, wherein the threshold signal generator comprises:
an upper resistive component coupled between a first potential node and an output node of the threshold signal generator;
a bipolar junction transistor having a base coupled to the output node of the threshold signal generator, a collector coupled to the output node of the threshold signal generator, and an emitter coupled to a second potential node through at least one resistive element; and
at least one resistive element coupled in parallel with the bipolar junction transistor, each having an input coupled to the collector of the bipolar junction transistor and an output coupled to the emitter of the bipolar junction transistor.

2. The pulse generator of claim 1, wherein the second potential node is adapted to receive a lower potential than the first potential node.

3. The pulse generator of claim 1, wherein the second potential node is adapted to receive a higher potential than the first potential node.

4. The pulse generator of claim 2, wherein the upper resistive component has a positive effective temperature coefficient of resistivity.

5. The pulse generator of claim 4, wherein the upper resistive component includes at least one resistive element, each resistive element having a positive effective temperature coefficient of resistivity.

6. The pulse generator of claim 5, wherein each resistive element is a semiconductor resistor.

7. The pulse generator of claim 1, further comprising at least one resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node.

8. The pulse generator of claim 2, further comprising:
a resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node through a selective coupling device, wherein the selective coupling device is selectively activated in response to a control signal.

9. The pulse generator of claim 8, wherein the selective coupling device is an n-channel field effect transistor.

10. The pulse generator of claim 1, wherein the second potential node is adapted to receive a lower potential than the first potential node, wherein the upper resistive component has a positive effective temperature coefficient of resistivity, the pulse generator further comprising:
a resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node through a selective coupling device, wherein the selective coupling device is selectively activated in response to a control signal.

11. The pulse generator of claim 10, wherein the at least one resistive element coupled in parallel with the bipolar junction transistor and the resistive element coupled in

series with the bipolar junction transistor each include at least one semiconductor resistor.

12. A pulse generator having a comparator whose output is generated in response to a difference between a potential level of a ramp signal from a ramp signal generator and a potential level of a threshold signal from a threshold signal generator, wherein the threshold signal generator comprises:

an upper resistive component coupled between a first potential node and an output node of the threshold signal generator and having a positive effective temperature coefficient of resistivity;

a bipolar junction transistor having a base coupled to the output node of the threshold signal generator, a collector coupled to the output node of the threshold signal generator, and an emitter coupled to a second potential node through at least one resistive element;

at least one resistive element coupled in parallel with the bipolar junction transistor, each having an input coupled to the collector of the bipolar junction transistor and an output coupled to the emitter of the bipolar junction transistor; and

at least one resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node.

13. The pulse generator of claim 12, wherein the second potential node is adapted to receive a lower potential than the first potential node.

14. The pulse generator of claim 12, wherein the upper resistive component includes at least one resistive element, each resistive element having a positive effective temperature coefficient of resistivity.

15. The pulse generator of claim 14, wherein each resistive element is a semiconductor resistor.

16. The pulse generator of claim 12, wherein the second potential node is adapted to receive a lower potential than the first potential node and wherein a resistive element coupled in series with the bipolar junction transistor has its output coupled to the second potential node through a selective coupling device, the selective coupling device being selectively activated in response to a control signal.

17. The pulse generator of claim 16, wherein the selective coupling device is an n-channel field effect transistor.

18. The pulse generator of claim 12, wherein the at least one resistive element coupled in parallel with the bipolar junction transistor and the at least one resistive element coupled in series with the bipolar junction transistor each include at least one semiconductor resistor.

19. A flash memory device, comprising:
a memory array of floating-gate memory cells;
a command control circuit for generating control signals to control operations on the memory array, the command control circuit including a pulse generator having a comparator whose output is generated in response to a difference between a potential level of a ramp signal from a ramp signal generator and a potential level of a threshold signal from a threshold signal generator, wherein the threshold signal generator comprises:
an upper resistive component coupled between a first potential node and an output node of the threshold signal generator;
a bipolar junction transistor having a base coupled to the output node of the threshold signal generator, a collector coupled to the output node of

the threshold signal generator, and an emitter coupled to a second potential node through at least one resistive element; and

at least one resistive element coupled in parallel with the bipolar junction transistor, each having an input coupled to the collector of the bipolar junction transistor and an output coupled to the emitter of the bipolar junction transistor.

20. The flash memory of claim 19, wherein the second potential node is adapted to receive a lower potential than the first potential node.

21. The flash memory of claim 19, wherein the second potential node is adapted to receive a higher potential than the first potential node.

22. The flash memory of claim 20, wherein the upper resistive component has a positive effective temperature coefficient of resistivity.

23. The flash memory of claim 22, wherein the upper resistive component includes at least one resistive element, each resistive element having a positive effective temperature coefficient of resistivity.

24. The flash memory of claim 23, wherein each resistive element is a semiconductor resistor.

25. The flash memory of claim 19, further comprising at least one resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node.

26. The flash memory of claim 20, further comprising:

a resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node through a selective coupling device, wherein the selective coupling device is selectively activated in response to a control signal.

27. The flash memory of claim 26, wherein the selective coupling device is an n-channel field effect transistor.

28. The flash memory of claim 19, wherein the second potential node is adapted to receive a lower potential than the first potential node, wherein the upper resistive component has a positive effective temperature coefficient of resistivity, the flash memory further comprising:

a resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node through a selective coupling device, wherein the selective coupling device is selectively activated in response to a control signal.

29. The flash memory of claim 28, wherein the at least one resistive element coupled in parallel with the bipolar junction transistor and the resistive element coupled in series with the bipolar junction transistor each include at least one semiconductor resistor.

30. A flash memory device, comprising:

a memory array of floating-gate memory cells;

a command control circuit for generating control signals to control operations on the memory array, the command control circuit including a pulse generator having a comparator whose output is generated in response to a difference

between a potential level of a ramp signal from a ramp signal generator and a potential level of a threshold signal from a threshold signal generator, wherein the threshold signal generator comprises:

an upper resistive component coupled between a first potential node and an output node of the threshold signal generator and having a positive effective temperature coefficient of resistivity;

a bipolar junction transistor having a base coupled to the output node of the threshold signal generator, a collector coupled to the output node of the threshold signal generator, and an emitter coupled to a second potential node through at least one resistive element;

at least one resistive element coupled in parallel with the bipolar junction transistor, each having an input coupled to the collector of the bipolar junction transistor and an output coupled to the emitter of the bipolar junction transistor; and

at least one resistive element coupled in series with the bipolar junction transistor, having an input coupled to the emitter of the bipolar junction transistor and an output coupled to the second potential node.

31. The flash memory of claim 30, wherein the second potential node is adapted to receive a lower potential than the first potential node.

32. The flash memory of claim 30, wherein the upper resistive component includes at least one resistive element, each resistive element having a positive effective temperature coefficient of resistivity.

33. The flash memory of claim 32, wherein each resistive element is a semiconductor resistor.

34. The flash memory of claim 31, wherein a resistive element coupled in series with the bipolar junction transistor has its output coupled to the second potential node through a selective coupling device, the selective coupling device being selectively activated in response to a control signal.

35. The flash memory of claim 34, wherein the selective coupling device is an n-channel field effect transistor.

36. The flash memory of claim 30, wherein the at least one resistive element coupled in parallel with the bipolar junction transistor and the at least one resistive element coupled in series with the bipolar junction transistor each include at least one semiconductor resistor.